(12) UK Patent Application (19) GB (11) 2 332 980 (13) A

(43) Date of A Publication 07.07.1999

(21) Application No 9808827.1

(22) Date of Filing 24.04.1998

(30) Priority Data
(31) 9782126 (32) 31.12.1997 (33) KR

(71) Applicant(s)
Samsung Electronics Co Limited
(Incorporated in the Republic of Korea)
416 Maetan-dong, Paldal-gu, Suwon-city,
Kyungki-do, Republic of Korea

(72) Inventor(s)
Sang-bom Kang
Yun-sook Chae
Chang-soo Park
Sang-in Lee

(74) Agent and/or Address for Service
Elkington and Fife
Prospect House, 8 Pembroke Road, SEVENOAKS,
Kent, TN13 1XR, United Kingdom

(51) INT CL[6]
H01L 21/285

(52) UK CL (Edition Q)
H1K KHABX K1CA K4C3G K4FU3 K4F20 K4F25 K4F26
K4F29
C7F FHB FHE FQ832 FQ841 FQ842 FQ887 FR861 F809

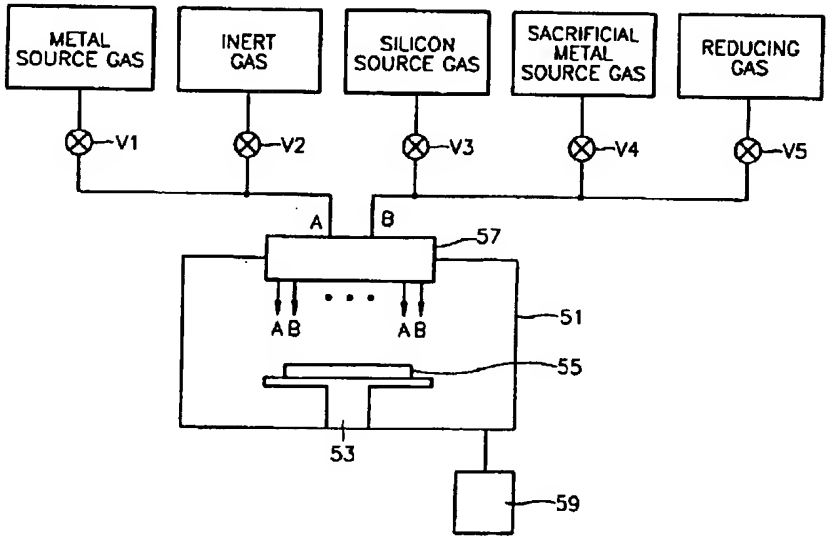
(56) Documents Cited
US 5405806 A

(58) Field of Search
UK CL (Edition P) C7F FACE FACX FAXE FAXX FCD ,
H1K KHABX KHAC KHAX
INT CL[6] H01L
ON LINE,W.P.I.

(54) A method for forming a conductive layer on a semiconductor substrate

(57) A sacrificial metal layer e.g. of aluminium is formed on a semiconductor substrate 55 by reacting a precursor such as trimethylaluminium with a reducing gas such as hydrogen and a metal layer, formed by metal atoms such as titanium dissociated from a metal halide gas such as titanium chloride, is deposited on the semiconductor substrate by reacting the sacrificial metal layer with the metal halide gas. Also, a silicon layer may be additionally formed on the metal layer using a silicon source gas, to thereby alternately stack metal layers and silicon layers.

FIG. 5



GB 2 332 980 A

FIG. 1

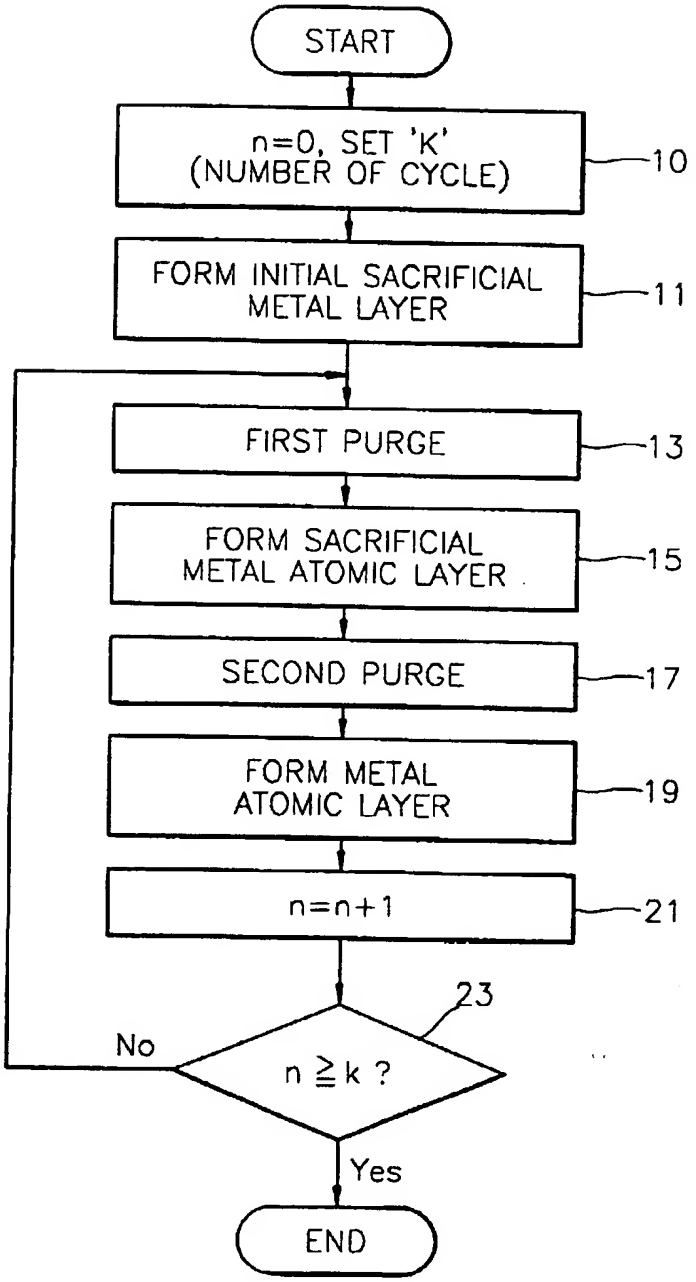

START
n=0, SET 'K' (NUMBER OF CYCLE)
10
FORM INITIAL SACRIFICIAL METAL LAYER
11
FIRST PURGE
13
FORM SACRIFICIAL METAL ATOMIC LAYER
15
SECOND PURGE
17
FORM METAL ATOMIC LAYER
19
n=n+1
21
23
No
n ≧ k ?
Yes
END

FIG. 2

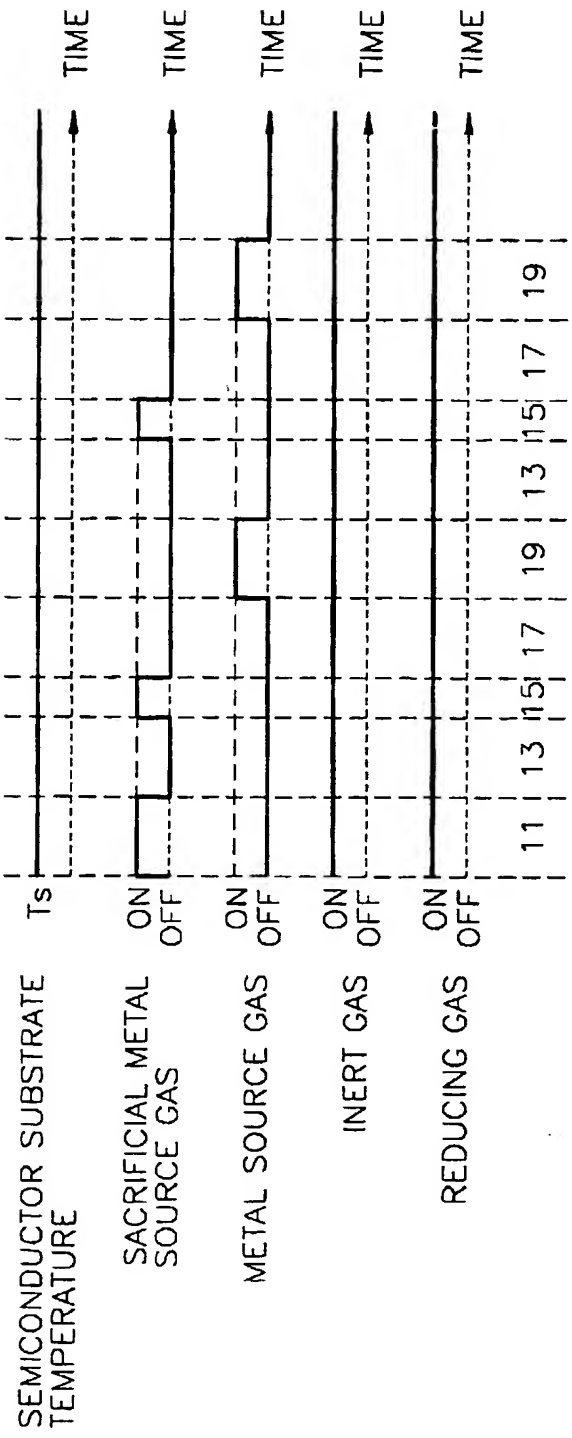

SEMICONDUCTOR SUBSTRATE TEMPERATURE
Ts
TIME
SACRIFICIAL METAL SOURCE GAS
ON
OFF
TIME
METAL SOURCE GAS
ON
OFF
TIME
INERT GAS
ON
OFF
TIME
REDUCING GAS
ON
OFF
TIME
11
13
15
17
19
13
15
17
19

FIG. 3

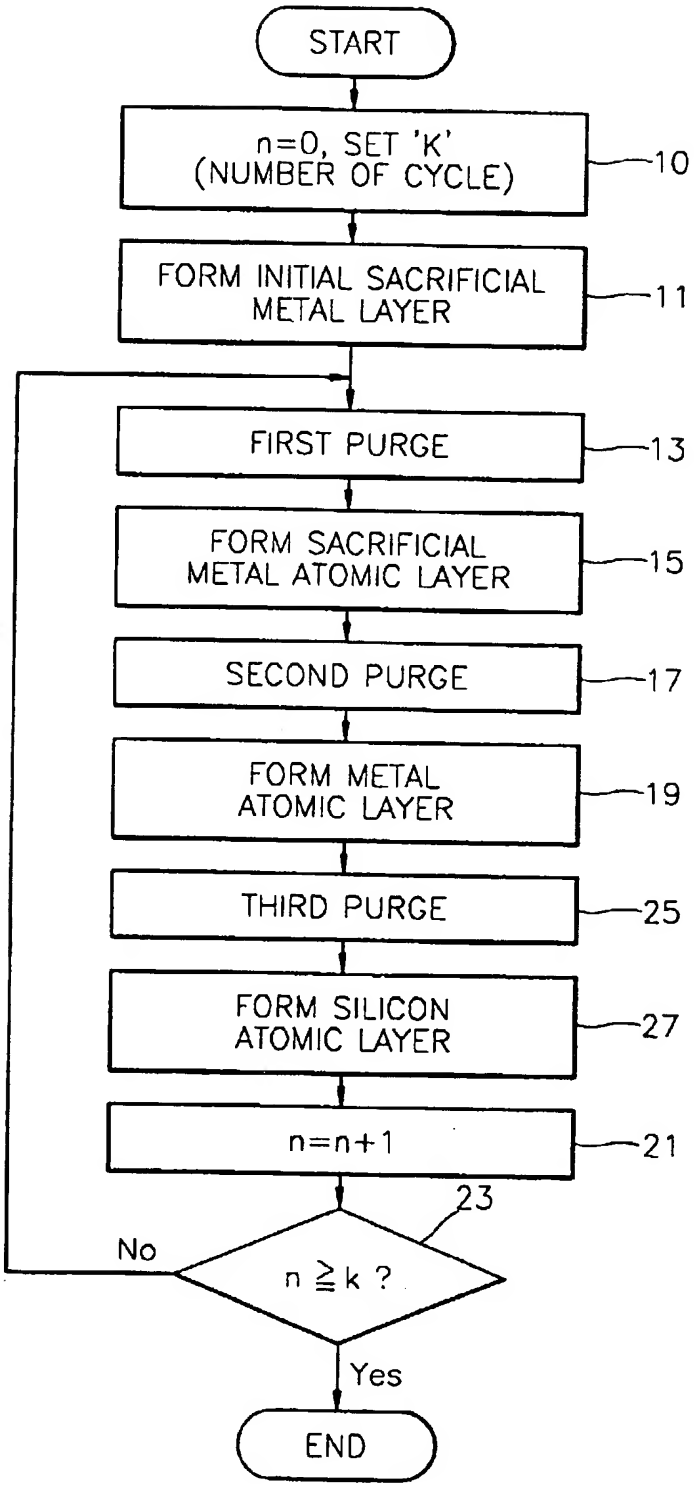

START
n=0, SET 'K' (NUMBER OF CYCLE)
10
FORM INITIAL SACRIFICIAL METAL LAYER
11
FIRST PURGE
13
FORM SACRIFICIAL METAL ATOMIC LAYER
15
SECOND PURGE
17
FORM METAL ATOMIC LAYER
19
THIRD PURGE
25
FORM SILICON ATOMIC LAYER
27
n=n+1
21
23
n ≧ k ?
No
Yes
END

FIG. 4

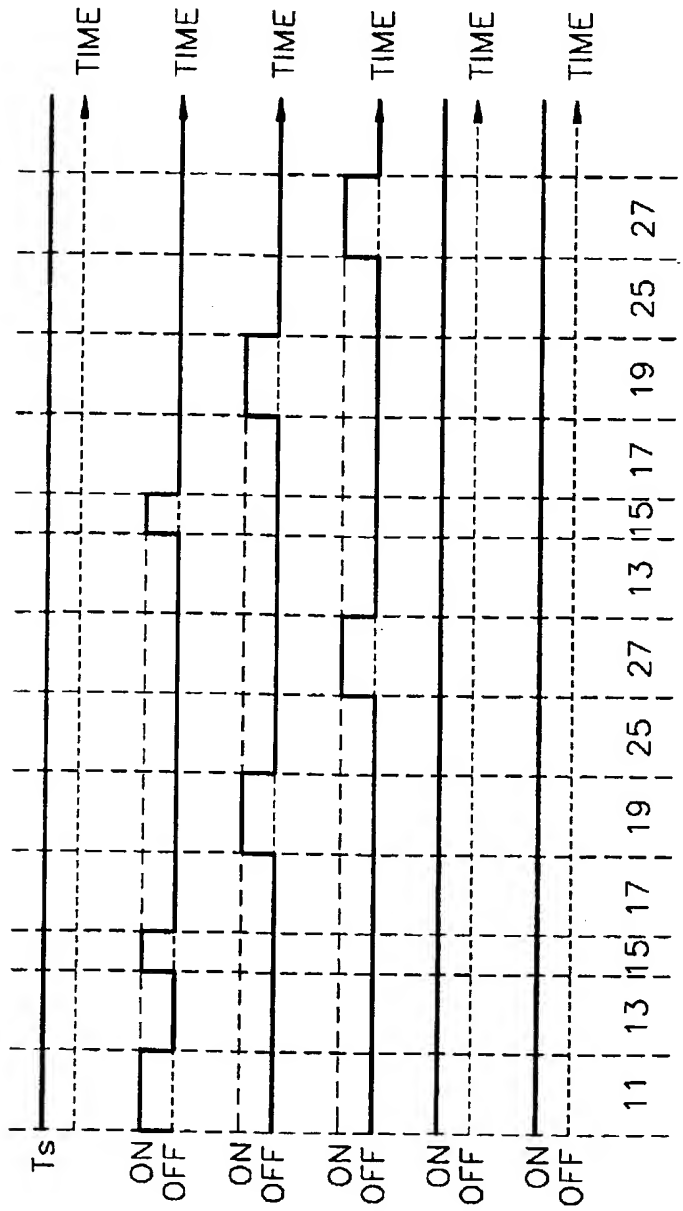

SEMICONDUCTOR SUBSTRATE TEMPERATURE
SACRIFICIAL METAL SOURCE GAS
METAL SOURCE GAS
SILICON SOURCE GAS
INERT GAS
REDUCING GAS
Ts
ON
OFF
TIME
11
13
15
17
19
25
27

FIG. 5

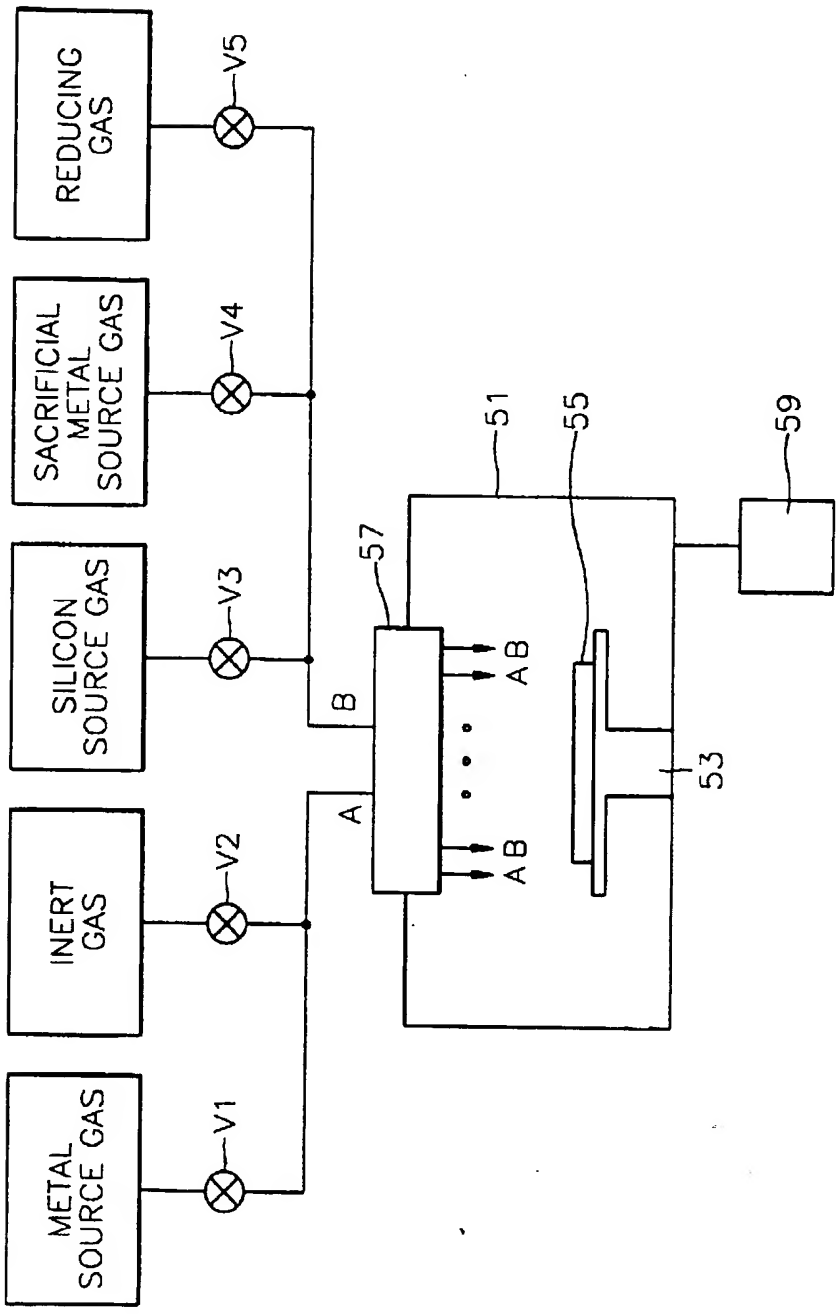

METAL SOURCE GAS
INERT GAS
SILICON SOURCE GAS
SACRIFICIAL METAL SOURCE GAS
REDUCING GAS
V1
V2
V3
V4
V5
A
B
57
A B
A B
51
55
53
59

FIG. 6

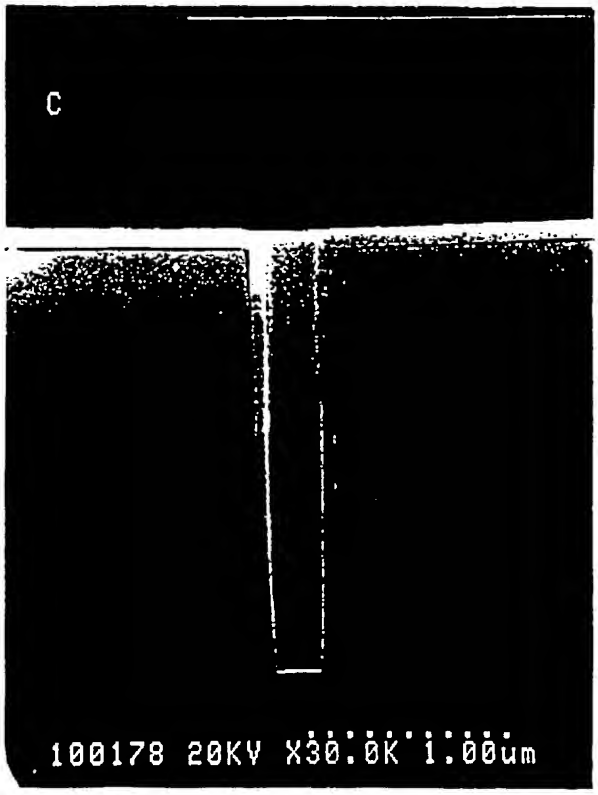
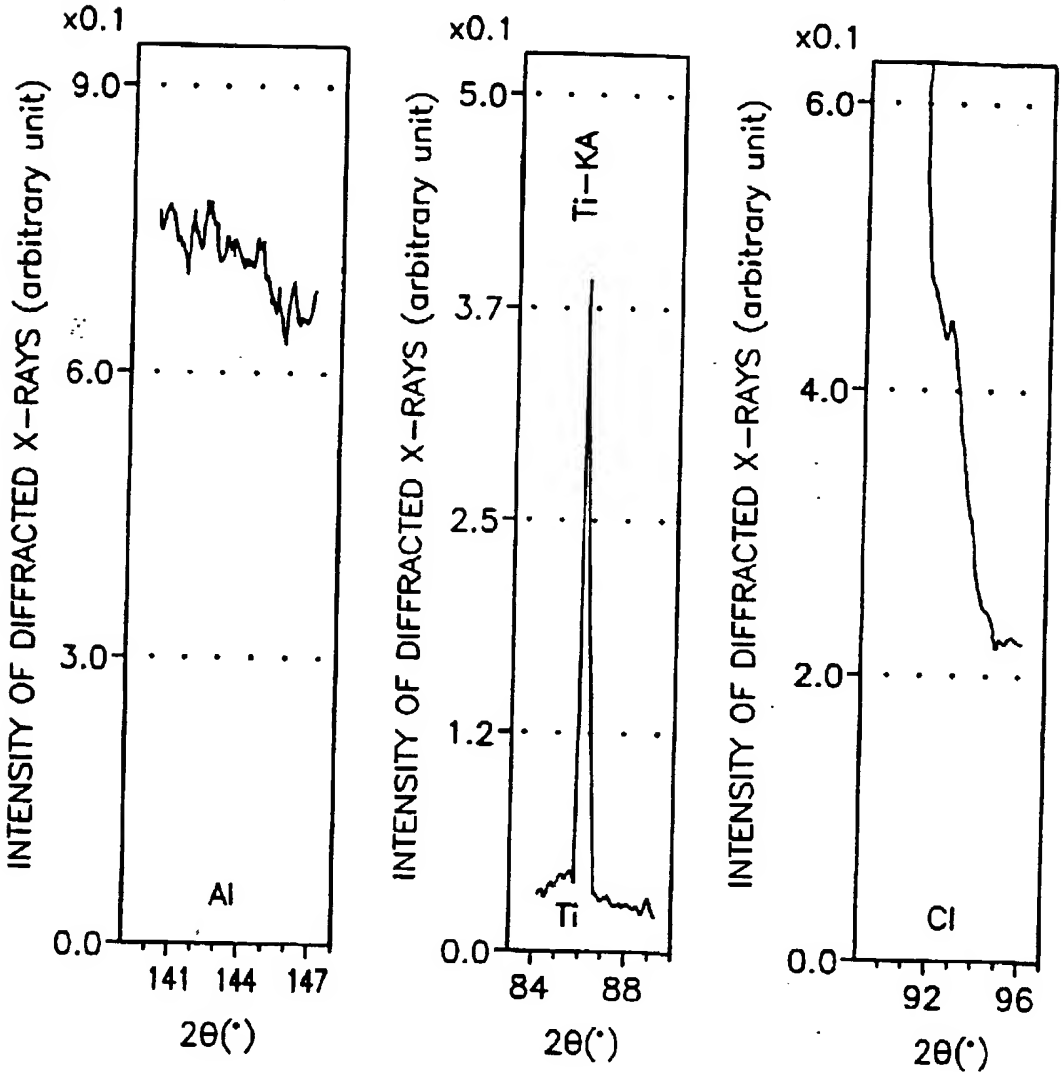


FIG. 7


x0.1
9.0
6.0
3.0
0.0
INTENSITY OF DIFFRACTED X-RAYS (arbitrary unit)
Al
141 144 147
2θ(°)
x0.1
5.0
3.7
2.5
1.2
0.0
Ti-KA
Ti
84 88
2θ(°)
x0.1
6.0
4.0
2.0
0.0
Cl
92 96
2θ(°)

A METHOD FOR FORMING A CONDUCTIVE LAYER USING AN ATOMIC LAYER DEPOSITION PROCESS

The present invention relates to a method for forming a conductive layer of a semiconductor device, and more particularly, to a method for forming a conductive layer using an atomic layer deposition process.

As the integration of a semiconductor device increases, the design rule is reduced. Thus, the aspect ratio of a contact hole becomes higher, but the junction depth becomes shallower. The junction depth directly depends on short channel effect of a MOS transistor. That is, a MOS transistor appropriate for a highly-integrated semiconductor device requires a short channel length, and a depth of a shallow source/drain region, i.e., the junction depth, must be shallow to improve the characteristics of the MOS transistor having the short channel. An interconnection technology for contacting the shallow junction with a metal interconnection requires a barrier metal layer. This prevents the metal interconnection from penetrating into the shallow junction, i.e., prevents a junction spiking phenomenon. A titanium nitride (TiN) layer is widely used for the barrier metal layer, and an ohmic layer, e.g., a titanium silicide layer, is interposed between the barrier metal layer and the junction. The titanium silicide layer having a melting point of 1540°C, a resistivity of 13 ~ 16 $\mu\Omega$-cm and a barrier height of 0.6eV with respect to an N-type impurity layer, is widely used for the ohmic layer or the interconnection. The titanium silicide layer used for the ohmic layer is formed by forming a titanium layer on the junction, i.e., a silicon substrate (impurity layer) doped with an impurity, and then annealing to react the titanium layer and the silicon substrate with each other.

As described above, in a conventional method for forming the metal interconnection, an interdielectric layer is formed on an impurity layer, and the interdielectric layer is patterned to form a contact hole exposing a predetermined region of the impurity layer. Also, the ohmic layer, the barrier metal layer and the metal interconnection are formed in sequence on the entire surface of the resultant structure where the contact hole is formed. Here, the ohmic layer can be obtained by forming a titanium layer on the exposed impurity layer and annealing the titanium layer, or forming the titanium silicide layer directly on the impurity layer. The titanium silicide layer must be formed at a low temperature enough to suppress damage of the impurity layer. Thus, there has been proposed a method for forming a titanium silicide layer using a plasma-enhanced chemical vapor deposition (PECVD) process, in "Plasma Enhanced CVD of Blanket $TiSi_2$ on Oxide Patterned Wafer" by J. Lee et al., J. Electrochem. Soc., vol. 139, No. 4, 1992, pp.1159 - 1165, and in "Material characterization of plasma-enhanced CVD titanium silicide" by Alan E. Morgan et al., J. Vac. Sci. Technol. B4(3), 1986, pp. 723 - 731. However, when the titanium silicide layer is formed on the contact hole having a high aspect ratio in a highly-integrated semiconductor device, the titanium silicide layer shows poor step coverage due to the plasma characteristic. Meanwhile, a method for forming a titanium silicide layer using a low pressure CVD (LPCVD) process at 600°C or higher has been proposed by V. Ilderem et al. and G. J. Reynolds et al. (see "Optimized Deposition Parameters for Low pressure CVD titanium silicide, J. Electrochem. Soc., 1988, pp. 2590 - 2596 and Selective titanium disilicide by Low Pressure CVD", J. Appl. Phys. 65(8), 1989, pp. 3212 - 3218). However, when the titanium silicide layer is formed at 600°C or higher, silicon consumption of the impurity layer contacting the titanium layer is increased, to thereby deteriorate junction leakage current characteristic. Thus, it is

difficult to adapt the titanium silicide layer through LPCVD for a highly-integrated semiconductor device requiring a shallow junction.

According to one aspect of the present invention, a method for forming a metal layer comprises the steps of a method for forming a metal layer, comprising the steps of:

(a) forming a sacrificial metal atomic layer on a semiconductor substrate;

(b) removing the sacrificial metal atomic layer and concurrently forming a metal atomic layer on the semiconductor substrate by reacting the sacrificial metal atomic layer with a metal halide gas; and,

(c) stacking a plurality of metal atomic layers on the semiconductor substrate by alternately forming the sacrificial atomic layer and the metal atomic layer, at least once.

The sacrificial metal atomic layer and the metal atomic layer are formed in sequence at least once on an initial metal atomic layer, which is the metal atomic layer initially formed on the semiconductor substrate, to thereby form a metal layer consisting of a plurality of metal atomic layers on the semiconductor substrate. Here, the initial sacrificial metal atomic layer, which is the sacrificial metal atomic layer initially formed on the semiconductor substrate, must be formed such that the entire surface of the exposed impurity layer is completely covered. If the surface of the impurity layer exposed by the contact hole is not completely covered with the initial sacrificial metal atomic layer, the metal halide gas reacts with and damages the impurity layer. Thus, an initial sacrificial metal layer covering the entire surface of the impurity layer completely, may be formed prior to forming the initial sacrificial metal atomic layer. At this time, preferably, while the initial sacrificial metal layer is formed, the semiconductor substrate is heated to 300 ~ 500°C. The initial sacrificial metal layer is formed of the same

material layer as the sacrificial metal atomic layer. The initial sacrificial metal layer or the sacrificial metal atomic layer is formed by reacting the sacrificial metal source gas and a reducing gas with each other. Here, preferably, H_2 gas or SiH_4 gas is used for the reducing gas.

Meanwhile, the metal halide gas must have a Gibbs free energy lower than that of a composition including a metal atom of the sacrificial metal atomic layer and a halogen atom of the metal halide gas. In other words, the metal atoms of the sacrificial metal atomic layer must be capable of being combined with halogen atoms instead of the combination of the metal atoms of the metal halide with halogen atoms. For instance, in order to form the metal atomic layer formed of titanium on the semiconductor substrate, preferably the metal halide employs $TiCl_4$ gas, TiI_4 gas, $TiBr_4$ gas or TiF_4 gas. At this time, if the metal halide is $TiCl_4$ gas, then preferably the sacrificial metal atomic layer is an Al layer, a La layer, a Pr layer, an In layer, a Ce layer, a Nd layer or a Be layer. This is because the Gibbs free energy of $TiCl_4$ gas is lower than that of Al_2Cl_6, $LaCl_3$ gas, $PrCl_3$ gas, In_2Cl_6 gas, $CeCl_3$ gas, $NdCl_3$ gas or Be_2Cl_4 gas. Similarly, if the TiI_4 gas is used for the metal halide in order to form a metal atomic layer formed of titanium on the semiconductor substrate, then preferably, the sacrificial metal atomic layer is an Al layer, a Zr layer or a Hf layer. This is because the Gibbs free energy of TiI_4 gas is lower than that of Al_2I_6 gas, ZrI_4 gas or HfI_4 gas.

Various metal halide gases, e.g., $TaCl_5$ gas, TaI_5 gas, $TaBr_5$ gas, TaF_5 gas, $HfCl_4$ gas, HfI_4 gas, $HfBr_4$ gas, HfF_4 gas, $ZrCl_4$ gas, ZrI_4 gas, $ZrBr_4$ gas or ZrF_4 gas may be used according to the kind of metal atomic layer to be formed on the semiconductor substrate.

As described above, if the metal halide gas is supplied to the surface of the resultant structure where the sacrificial metal atomic layer is formed or where the initial sacrificial metal layer and the initial sacrificial metal atomic layer are formed, then metal atoms in the sacrificial metal atomic layer and the metal atoms in the initial sacrificial metal layer combine with the halogen atoms of the metal halide gas, to thereby generate a volatile gas. Thus, the metal atoms in the metal halide, e.g., transition metal atoms, are deposited on the semiconductor substrate, to form a metal atomic layer. Preferably, the sacrificial metal atomic layer and the metal atomic layer are formed in sequence when the semiconductor substrate is heated to 300 ~ 500°C.

According to another aspect of the present invention, a sacrificial metal atomic layer and a metal atomic layer are formed on a semiconductor substrate in the same manner as in the first aspect, and a silicon atomic layer is formed on the metal atomic layer. Here, an initial sacrificial metal layer can be formed on the semiconductor substrate like the first aspect, before an initial sacrificial metal atomic layer, which is a layer initially formed on the semiconductor substrate, is formed. Next, the sacrificial metal atomic layer, the metal atomic layer and a silicon atomic layer are stacked in sequence on the resultant structure where the initial silicon atomic layer is formed, at least once, to thereby alternately stack a plurality of metal atomic layers and a plurality of silicon atomic layers on the semiconductor substrate. At this time, when the thickness of a metal atomic layer and the thickness of a silicon atomic layer are appropriately controlled, a metal silicide layer having a desired composition ratio may be formed. Alternatively, the silicon atomic layer and the metal atomic layer are formed in sequence at least once on the semiconductor substrate, to thereby alternately stack a plurality of silicon atomic layers and a plurality of metal atomic layers. Then, the resultant structure where the plurality of

silicon atomic layers and the plurality of metal atomic layers are alternately stacked is annealed if necessary, to form a metal silicide layer capable of improving contact resistance. Preferably, the annealing is performed through a rapid thermal process (RTP), a furnace annealing process or a vacuum annealing process. While the silicon atomic layer is formed, the semiconductor substrate is heated to 300 ~ 500°C. The silicon atomic layer is formed using a silicon source gas. i.e., a precursor containing silicon atoms. Preferably, the silicon source gas employs SiH_4 gas, Si_2H_6 gas, $(CH_3)_3SiC{\equiv}CSi(CH)_3$ gas, $((CH_3)_3Si)_2CH_2$ gas, $(CH_3)_3CSi(CH_3)_2Cl$ gas, $(C_4H_9)SiCl_3$ gas, $(CH_3)_3SiN(C_2H_5)_2$ gas, $(CH_3)_2SiCl_2$ gas, $((CH_3)_2Si\text{-})_n$ gas, $(C_6H_5)_2SiCl_2$ gas, $(C_6H_5)_2SiH_2$ gas, $C_2H_5SiCl_3$ gas, $Cl_3SiSiCl_3$ gas, $(CH_3)_3SiSi(CH_3)_3$ gas, CH_3SiCl_2H gas, $(CH_3)(C_6H_5)SiCl_2$ gas, $C_6H_5SiCl_3$ gas, $SiBr_4$ gas, $SiCl_4$ gas, SiF_4 gas, SiI_4 gas, $(C_{32}H_{16}N_8)SiCl_2$ gas, $Si(Si(CH_3)_3)_4$ gas, $Si(CH_3)_4$ gas, CH_3SiCl_3 gas, $HsiCl_3$ gas, $(C_2H_5)_2SiCl$ gas, $CF_3Si(CH_3)_3$ gas, $(CH_3)_3SiCl$ gas, $(CH_3)_3SiH$ gas, $(CH_3)_2SiC{\equiv}CH$ gas, $(C_5H_5)Si(CH_3)_3$ gas, $(C_5(CH_3)_5)Si(CH_3)_3$ gas, $(C_6H_5)_3SiCl$ gas, $(C_6H_5)_3SiH$ gas, $((CH_3)_2N)_3CH$ gas or $CH_2{=}CHSiCl_3$ gas.

In the present invention, a metal layer or a metal silicide layer having excellent step coverage may be formed at 500°C or lower on the surface of the semiconductor substrate having a contact hole with a high aspect ratio. Thus, in manufacturing a highly-integrated semiconductor device requiring a shallow junction, a conductive layer having excellent reliability, i.e., a barrier metal layer or an ohmic layer having excellent reliability, may be formed.

Examples of the present invention will now be described in detail with reference to the accompanying drawings, in which:

FIG. 1 is a flowchart illustrating the process sequence of one embodiment of the present invention;

FIG. 2 is a timing diagram illustrating one embodiment of the present invention;

FIG. 3 is a flowchart illustrating the process sequence of another embodiment of the present invention;

FIG. 4 is a timing diagram illustrating another embodiment of the present invention;

FIG. 5 is a schematic view of an apparatus for forming a conductive layer used for embodiments of the present invention;

FIG. 6 is a scanning electron microscope (SEM) photograph of a cross-section of a titanium layer according to one embodiment of the present invention; and,

FIG. 7 shows components of the titanium layer of FIG. 6 measured by X-ray fluorescence analysis.

Referring to FIG. 5, an apparatus used to form a conductive layer according to the present invention includes a reaction chamber 51, a susceptor 53 installed on the bottom of the reaction chamber 51 to locate a semiconductor substrate 55 thereon, a shower head 57 installed over the susceptor 53 to inject a reaction gas into the reaction chamber 51, and a vacuum pump 59 connected to the reaction chamber 51 to control the pressure in the reaction chamber 51. Here, the shower head 57 includes two gas inlets A and B separated from each other. A metal source gas and an inert gas are injected into the reaction chamber 51 through the gas inlet A, and a silicon source gas, a sacrificial metal source gas and a reducing gas are injected into the reaction chamber 51 through the gas inlet B. This is to suppress the reaction of gases in one of the inlets A and B before arriving in the chamber 51. The injection of the metal source gas and the inert gas into the gas inlet A is controlled by first and second valves V1 and V2 respectively, and the

injection of the silicon source gas, the sacrificial metal source gas and the reducing gas into the gas inlet B is controlled by third, fourth and fifth valves V3, V4 and V5 respectively.

In one embodiment of the present invention, described with reference to FIGS. 1, 2 and 5, a junction doped with an impurity, i.e., an impurity layer, is formed on the semiconductor substrate, e.g., the surface of a predetermined region of a silicon substrate. The impurity layer which corresponds to a source/drain region of a MOS transistor must be formed to the depth of 0.1μm or less for a highly integrated semiconductor device. This is because the short channel effect of the MOS transistor is closely related to the junction depth. That is, as the junction depth of the impurity layer is shallower, the short channel effect of the MOS transistor is improved. An interdielectric layer is formed on the entire surface of the resultant structure where the impurity layer is formed, and the interdielectric layer is patterned to form a contact hole exposing a predetermined region of the impurity layer. At this time, as the integration of the semiconductor device is increased, the thickness of the interdielectric layer is increased and the diameter of the contact hole is reduced. Thus, as the integration of the semiconductor device is increased, the aspect ratio of the contact hole is increased. The semiconductor substrate 55 where the contact hole is formed is loaded on the susceptor 53 installed in the reaction chamber of the apparatus for forming a conductive layer. Also, in a process recipe, a value n is initialized to zero and at the same time the value k indicating the number of desired process cycle is determined (step 10).

Subsequently, if the temperature Ts of the semiconductor substrate 55 is controlled to 300 ~ 550°C, second, fourth and fifth valves V2, V4 and V5 are opened, so that the inert gas, the sacrificial metal source gas and the reducing gas are injected into the chamber 51

for a predetermined time, to thereby form an initial sacrificial metal layer on the entire surface of the semiconductor substrate 55 where the contact hole is formed (step 11). The sacrificial metal source gas and the reducing gas mix with each other in the gas inlet B, but do not react with each other due to the low temperature in the gas inlet B of 100 ~ 150°C. At this time, the pressure in the reaction chamber 51 is controlled to 10 torr or below. Preferably, the initial sacrificial metal layer is a metal layer capable of easily reacting with a metal source gas used to form a desired metal atomic layer in a subsequent process, i.e., a metal-halide gas consisting of a transition metal and a halogen element. For instance, in order to form the titanium metal atomic layer, preferably a metal halide containing titanium, i.e., a $TiCl_4$ gas, a TiI_4 gas, a $TiBr_4$ gas, or a TiF_4 gas is desirable for the metal halide gas. Also, if the $TiCl_4$ gas is used for the metal halide gas, an Al layer, a La layer, a Pr layer, an In layer, a Ce layer, a Nd layer or a Be layer are desirable for the initial sacrificial metal layer. At this time, the Al layer is most preferable for the initial sacrificial metal layer. This is because aluminum has the highest Gibbs free energy with respect to Cl as shown in Table 1a and various precursors. Preferably, argon gas or nitrogen gas are used for the inert gas, and hydrogen gas is used for the reducing gas. The reducing gas reduces the sacrificial metal source gas. The Gibbs free energy with respect to various metal halide gases at an absolute temperature of 700°K (427°C) is shown in Tables 1a, 1b, 2, 3 and 4.

(Table 1a)

Gibbs free energy of various metal halide gases containing chlorine at 427°C

Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)
Al_2Cl_6	-1121.9	$HfCl_3$	-626.7	$BeCl_2$	-373.1
$ThCl_4$	-895.8	$EuCl_3$	-621.6	BCl_3	-367.7
UCl_5	-811.9	$YbCl_3$	-621.5	$SiCl_3$	-365.7
$HfCl_4$	-804.7	K_2Cl_2	-609.8	$SnCl_4$	-362.3
$ZrCl_4$	-777.6	Rb_2Cl_2	-607.6	$InCl_3$	-335.8
$LaCl_3$	-708.9	Li_2Cl_2	-597.8	$AlCl_2$	-305.5
$PrCl_3$	-706.9	$SiCl_4$	-569.6	$TaCl_3$	-300.1
In_2Cl_6	-703.7	$AlCl_3$	-550.1	$GeCl_3$	-299.8
$CeCl_3$	-699.5	Fe_2Cl_6	-526.8	$MnCl_2$	-286.4
$NdCl_3$	-696.6	$BaCl_2$	-524.3	WCl_5	-285.6
Be_2Cl_4	-692.6	$SrCl_2$	-498.1	CsCl	-276.7
$TiCl_4$	-678.3	$TaCl_4$	-497.5	$ZnCl_2$	-273.5
$GdCl_3$	-674.3	$CaCl_2$	-489.1	WCl_4	-267.6
$TbCl_3$	-668.1	$PbCl_4$	-462.1	Ti_2Cl_2	-259.8
$HoCl_3$	-659.7	$VaCl_4$	-447.2	$GaCl_2$	-258.4
$ErCl_3$	-651.7	$GeCl_4$	-410.8	$SbCl_5$	-249.9
Cs_2Cl_2	-644.1	$MgCl_2$	-407.8	Cu_3Cl_3	-242.9
$TmCl_3$	-641.5	Fe_2Cl_4	-406.5	PCl_5	-242.3
$TaCl_5$	-636.6	$GaCl_3$	-388.6	$FeCl_3$	-240.6

(Table 1b)

Gibbs free energy of various metal halide gases containing chlorine at 427°C

Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)
$InCl_2$	-240.2	CaCl	-165.1	$NiCl_2$	-101.8
$BiCl_3$	-238.5	$TeCl_4$	-136.4	HCl	-98.7
$AsCl_3$	-231.4	$HgCl_2$	-136.2	$SeCl_2$	-50.5
$SnCl_2$	-215.8	$TeCl_2$	-134.6	BiCl	-30.9
BaCl	-198.5	$CoCl_2$	-125.2	BeCl	-6.2
$SiCl_2$	-195.5	GaCl	-123.1	AgCl	29.6
SrCl	-181.5	AlCl	-111.6	BCl	74.3
$FeCl_2$	-174.5	BCl_2	-109.9	SiCl	123.7

(Table 2)

Gibbs free energy of various metal halide gases containing iodine at 427°C

Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)
ThI_4	-512	ZrI_4	-409	TiI_4	-320
Al_2I_6	-510	HfI_4	-405	PbI_4	-266
K_2I_2	-480	DyI_3	-402	MgI_2	-239
LaI_3	-457	TmI_3	-399	CuI	-237
PrI_3	-448	GdI_3	-388	CsI	-220
CeI_3	-442	BaI_2	-380	TaI_5	-202
NdI_3	-438	UI_4	-377	SiI_4	-150
Li_2I_2	-427	SrI_2	-353	HI	-11.8
ErI_3	-410	CaI_2	-338	-	-

(Table 3)

Gibbs free energy of various metal halide gases containing bromine at 427°C

Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)
Al_2Br_6	-860	$HoBr_3$	-567	$CaBr_2$	-435
Mg_2Br_4	-764	$ErBr_3$	-566	$PbBr_4$	-428
$ThBr_4$	-743	$TmBr_3$	-563	$TaBr_5$	-424
$HfBr_4$	-639	$TbBr_3$	-559	$EuBr_2$	-413
$ZrBr_4$	-627	$DyBr_3$	-559	$SiBr_4$	-387
$LaBr_3$	-621	$GdBr_3$	-551	Cu_3Br_3	-187
$CeBr_3$	-616	Li_2Br_2	-534	WBr_6	-139
$PrBr_3$	-612	$TiBr_4$	-527	HBr	-58.6
UBr_4	-602	Na_2Br_2	-510	-	-
$NdBr_3$	-598	$SrBr_2$	-453	-	-

(Table 4)

Gibbs free energy of various metal halide gases containing iodine at 427°C

Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)	Compound	Gibbs free energy (kJ/mol)
Al_2F_6	-2439	HfF_4	-1592	Li_3F_3	-1457
UF_6	-1958	ZrF_4	-1587	PrF_3	-1231
TaF_5	-1687	S_2F_{10}	-1581	AsF_5	-1080
ThF_4	-1687	SiF_4	-1515	CuF_2	-287.3
Mg_2F_4	-1624	WF_6	-1513	HF	-277.1
NbF_5	-1607	TiF_4	-1467	-	-

A metal source gas and an initial sacrificial metal layer appropriate for forming a desired metal atomic layer on a semiconductor substrate can be selected from Tables 1 through 4. For instance, in order to form a titanium atomic layer as a metal atomic layer, an Al layer, a La layer, a Pr layer, an In layer, a Ce layer, a Nd layer or a Be layer is desirable for the initial sacrificial metal layer, and a $TiCl_4$ gas is desirable for the metal source gas. Preferably, the sacrificial metal source gas for forming the Al layer as an initial sacrificial metal layer is a precursor containing Al, e.g., $(C_4H_9)_2AlH$, $(C_4H_9)_3AlH$, $(C_2H_5)_3Al$, $(CH_3)_3Al$, $AlH_3N(CH_3)_3$, $(CH_3)_2AlH$, or $(CH_3)_2C_2H_5N:AlH_3$. Also, it is preferable that the sacrificial metal source gas for forming the La layer as an initial sacrificial metal layer is a precursor containing La, e.g., $(C_5H_5)_3La$ or $(C_2H_7C_4H_4)_3La$, and the sacrificial metal source gas for forming the Pr layer as an initial sacrificial metal layer is a precursor containing Pr, such as $(C_5H_5)_3Pr$ or $(C_3H_7C_5H_4)_3$ Pr. Also, it is preferable that the sacrificial metal source gas for forming the In layer as an initial sacrificial metal layer is a precursor containing In, e.g., C_2H_5In, $(CH_3)_5C_5In$, $(C_2H_5)_3In$ or $(CH_3)_3In$. Also, it is preferable that the sacrificial metal source gas for forming the Ce layer as an initial sacrificial metal layer is a precursor containing Ce, e.g., $(C_5H_5)_3Ce$ or $((C_5H_5)C_5H_4)_3Ce$. It is preferable that the sacrificial metal source gas for forming the Nd layer as an initial sacrificial metal layer is a precursor containing Nd, e.g., $(C_5H_5)_3Nd$ or $(C_3H_7C_5H_4)_3Nd$. Furthermore, it is preferable that the sacrificial metal source gas for forming the Be layer as an initial sacrificial metal layer is a precursor containing Be, e.g., $Be(C_2H_5)_2$. The precursor containing Al is most preferable as the sacrificial metal source gas. This is because Al has a Gibbs free energy higher than any other transition element with halogen atoms, e.g., Cl, I, Br or F as shown in Tables 1 through 4, and various precursors as described above.

If the Al layer is formed for the initial sacrificial metal layer, TMA(trymethyl aluminum; $((CH_3)_3Al)$) is a typical precursor for the sacrificial metal source gas. At this time, the H_2 gas, which is the reducing gas, reacts with the TMA gas so that CH_3 of the TMA gas is changed to CH_4. The CH_4 is exhausted from the reaction chamber 51 and the Al atoms are deposited on the surface of the semiconductor substrate to form the Al layer. Subsequently, a peripheral portion of the resultant structure where the initial sacrificial metal layer is formed is purged by the inert gas to completely exhaust the sacrificial metal source gas remaining in the reaction chamber 51 (step 13), (a first purge process.) The reducing gas may be supplied during the first purge process. Also, the temperature of the semiconductor substrate is maintained at 300 ~ 500°C. Here, the temperature of the semiconductor substrate during forming the initial sacrificial metal layer may be controlled to be equal to or different from the temperature of the semiconductor substrate during the first purge process.

After completion of the first purge process, the sacrificial metal source gas, the reducing gas and the inert gas are injected into the reaction chamber 51 to react the sacrificial metal source gas with the reducing gas, so that a sacrificial metal atomic layer is formed on the initial sacrificial metal layer (step 15). For instance, if TMA$((CH_3)_3Al)$ gas and H_2 gas are used for the sacrificial metal source gas and the reducing gas, respectively, an Al layer is formed as a sacrificial metal atomic layer. Here, the sacrificial metal atomic layer is formed of the same material as the initial sacrificial metal layer. For instance, if the initial sacrificial metal layer is the Al layer, the sacrificial metal atomic layer is also formed of Al. Also, the sacrificial metal atomic layer is formed using the same sacrificial metal source gas as that used to form the initial sacrificial metal layer. At this time, preferably, the thickness of the sacrificial metal atomic layer is 4 ~ 5Å. Here, when the

entire surface of the exposed impurity layer is covered with the sacrificial metal atomic layer, the process of forming the initial sacrificial metal layer may be omitted. In other words, the initial sacrificial metal layer is for preventing the metal source gas injected into the reaction chamber 51 during formation of the metal atomic layer from reacting with silicon atoms in the impurity layer.

The peripheral portion of the resultant structure where the sacrificial metal layer is formed is purged with the inert gas to completely exhaust the sacrificial metal source gas remaining in the reaction chamber 51 (step 17), (a second purge process.) The reducing gas may be supplied during the second purge process. After completion of the second purge process, the metal source gas, the inert gas and the reducing gas are injected into the reaction chamber 51, to thereby remove the sacrificial metal atomic layer and the initial sacrificial metal layer and concurrently form a metal atomic layer on the entire surface of the semiconductor substrate (step 19). At this time, preferably, a metal halide gas containing metal atoms of a metal layer to be formed, e.g., $TiCl_4$, is used for the metal source gas. The inert gas, e.g., N_2 gas or Ar gas, is a carrier gas of the metal source gas, i.e., the metal halide gas. When both the sacrificial metal atomic layer and the initial sacrificial metal layer are an Al layer and $TiCl_4$ gas is used for the metal halide gas, Al_2Cl_6 gas is generated by combining Al atoms of the Al layer with Cl atoms of $TiCl_4$, and Ti atoms dissolved from the $TiCl_4$ gas are deposited on the semiconductor substrate to form a Ti layer. The Al_2Cl_6 gas is exhausted from the reaction chamber 51.

Since the Gibbs free energy of the Al_2Cl_6 is higher than that of the $TiCl_4$ gas as shown in Table 1A, the Al layer reacts with the $TiCl_4$ gas to form the Ti layer. $TaCl_5$ gas, $HfCl_4$ gas, $ZrCl_4$ gas, TiI_4 gas, TaI_5 gas, HfI_4 gas, ZrI_4 gas, $TiBr_4$ gas, $TaBr_5$ gas, $HfBr_4$ gas,

$ZrBr_4$ gas. TiF_4 gas, TaF_5 gas, HfF_4 gas or ZrF_4 gas may be used instead of the $TiCl_4$ gas for the metal halide gas. In order to form a Hf layer or a Zr layer using the $HfCl_4$ gas or the $ZrCl_4$ gas as the metal halide gas, the Al layer is optimum for the sacrificial metal atomic layer or the initial sacrificial metal layer. This is because the Gibbs free energies of $HfCl_4$ gas and $ZrCl_4$ gas are higher than that of $LaCl_3$ gas, $PrCl_3$ gas, In_2Cl_6 gas, $CeCl_3$ gas, $NdCl_3$ gas and Be_2Cl_4 gas as shown in Table 1A. Also, in order to form a desired metal atomic layer mostly using the metal halide gases, the Al layer is most preferable for the sacrificial metal atomic layer or the initial sacrificial metal layer as shown in Tables 2 to 4. It is preferable that steps 13, 15, 17 and 19 (the first purge, forming the sacrificial metal atomic layer, the second purge and forming the metal atomic layer) are formed at the same temperature. After forming the metal atomic layer, the value **n** is increased by 1 (step 21), and the increased number **n** is compared to the number **k** of initially predetermined cycles (step 23). If the increased **n** value is smaller than the number **k** of initially predetermined cycles, steps 13, 15, 17 and 19 (the first purge, forming the sacrificial metal atomic layer, the second purge and forming the metal atomic layer) are repeated in sequence until the value **n** is equal to the number **k** of cycles, to thereby form a metal layer of the desired thickness on the semiconductor substrate. When the resultant structure where the metal layer is formed is annealed at a predetermined temperature, a metal silicide layer is formed at an interface between an impurity layer and the metal layer. Here, the metal silicide layer is an ohmic layer improving contact resistance between the metal layer and the impurity layer.

The Ti layer formed according to one embodiment of the present invention is shown in FIG. 6. In FIG. 6, during forming an initial sacrificial metal layer, the first purge, forming the sacrificial metal atomic layer, the second purge and forming the metal atom

layer, the temperature 'Ts' of the semiconductor substrate was 450°C. The initial sacrificial metal layer was formed of the Al layer by reacting TMA gas with H_2 gas for about 10 sec. At this time, inert N_2 gas was also injected into the reaction chamber. The N_2 gas and the H_2 gas were injected into the reaction chamber at flow rates of 40 sccm and 1000 sccm, respectively, and the pressure in the reaction chamber was approximately 3 torr. Also, the TMA gas was generated using a bubbler at room temperature. At this time, no carrier gas was used for the TMA gas, so the TMA gas was injected into the reaction chamber by a difference between the vapor pressure of the TMA gas and the pressure in the reaction chamber. After forming the initial sacrificial metal layer (Al layer), the TMA gas was not supplied any more, and the first purge process was performed for about 5 sec in order to completely remove the TMA gas remaining in the reaction chamber. At this time, the N_2 gas and the H_2 gas were continuously injected to keep the pressure in the reaction chamber at approximately 8 torr. Then, after completing the first purge process, TMA gas was injected into the reaction chamber for approximately 1 sec, and thus the H_2 gas reacted with the TMA gas to form a thin sacrificial metal atomic layer, i.e., an Al atomic layer. Next, TMA gas was not supplied and second purge process was performed in the same manner as the first purge process. Then, $TiCl_4$ metal source gas was injected into the reaction chamber for approximately 5 sec, and thus the Al layer and the $TiCl_4$ gas reacted with each other, to form a Ti atomic layer on the entire surface of the semiconductor substrate. Subsequently, the steps of the first purge, forming the sacrificial metal atomic layer, the second purge and forming the metal atomic layer were repeated in sequence 50 times.

Referring to FIG. 6, it can be seen that the Ti layer according to one embodiment of the present invention was formed inside of the contact hole having an aspect ratio of 5 or

higher and on the peripheral portion of the contact hole to a uniform thickness of approximately 600 Å.

In FIG. 7, the horizontal axis represents a diffraction angle of X-rays, and the vertical axis represents the intensity of the diffracted X-rays in an arbitrary unit. Also, in the graph, the range of the diffraction angle 2θ of the X-ray between 140° and 170° is the result obtained by measuring an Al component, the range between 84° and 89° represents the result obtained by measuring a Ti component, and the range between 90° and 96° represents the result obtained by measuring a Cl component.

It can be seen from FIG. 7 that the Ti layer formed according to one embodiment of the present invention contains no impurity, only Ti atoms.

In FIGS. 3 and 4, portions represented by the same reference numerals as in the first embodiment refer to the same procedure.

Referring to FIGS. 3, 4 and 5, after steps 11, 13, 15, 17 and 19 of forming the initial sacrificial metal layer, the first purge, forming the sacrificial metal atomic layer, the second purge and forming the metal atomic layer, steps 25 and 27 of third purge and forming a silicon atomic layer are additionally performed, to thereby form a metal silicide layer. The third purge process 25 is performed in the same manner as the first and second purge processes 13 and 17. The silicon atomic layer is formed on a metal atomic layer by reacting the silicon source gas injected into the reaction chamber 51 after completion of the third purge process 25. At this time, during forming the silicon layer, the temperature of the semiconductor substrate is maintained at the same temperature as

in the third purge process 25, i.e., 300 ~ 500°C. Like in the first embodiment of the present invention, steps 13, 15, 17, 19, 25 and 27 (the first purge, forming the sacrificial metal atomic layer, the second purge, forming the metal atomic layer, the third purge and forming the silicon atomic layer) are repeated in sequence, as desired, and thus the metal atomic layer and the silicon atomic layer are alternately stacked. At this time, the metal atomic layer and the silicon atomic layer react with each other, and thus a metal silicide layer may be formed. The composition ratio of the metal silicide layer may be changed by controlling the thicknesses of the metal atomic layer and the silicon atomic layer. Preferably, the silicon source gas employs SiH_4 gas, Si_2H_6 gas, $(CH_3)_3SiC\equiv CSi(CH)_3$ gas, $((CH_3)_3Si)_2CH_2$ gas, $(CH_3)_3CSi(CH_3)_2$ Cl gas, $(C_4H_9)SiCl_3$ gas, $(CH_3)_3SiN(C_2H_5)_2$ gas, $(CH_3)_2SiCl_2$ gas, $((CH_3)_2Si-)_n$ gas, $(C_6H_5)_2SiCl_2$ gas, $(C_6H_5)_2SiH_2$ gas, $C_2H_5SiCl_3$ gas, $Cl_3SiSiCl_3$ gas, $(CH_3)_3SiSi(CH_3)_3$ gas, CH_3SiCl_2H gas, $(CH_3)(C_6H_5)SiCl_2$ gas, $C_6H_5SiCl_3$ gas, $SiBr_4$ gas, $SiCl_4$ gas, SiF_4 gas, SiI_4 gas, $(C_{32}H_{16}N_8)SiCl_2$ gas, $Si(Si(CH_3)_3)_4$ gas, $Si(CH_3)_4$ gas, CH_3SiCl_3 gas, $HsiCl_3$ gas, $(C_2H_5)_3SiCl$ gas, $CF_3Si(CH_3)_3$ gas, $(CH_3)_3SiCl$ gas, $(CH_3)_3SiH$ gas, $(CH_3)_3SiC\equiv CH$ gas, $(C_5H_5)Si(CH_3)_3$ gas, $(C_5(CH_3)_5)Si(CH_3)_3$ gas, $(C_6H_5)_3SiCl$ gas, $(C_6H_5)_3SiH$ gas, $((CH_3)_2N)_3CH$ gas or $CH_2=CHSiCl_3$ gas.